# AD6986D Datasheet

## Zhuhai Jieli Technology Co.,LTD

**Version：1.0**

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# AD6986D Features

## CPU

- 32-bit DSP supports hardware Float Point Unit(FPU)
- Up to 160MHz programmable processor
- 64Vectored interrupts
- 4 Levels interrupt priority

## DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC,AES)
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 20-band EQ configuration for voice Effects

## Audio Codec

- Two channels 24-bit DAC, SNR >= 101dB
- Two channels 24-bit ADC , SNR >= 92dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- One analog MIC amplifier, build-in MIC bias generator
- Supports two PDM digital MIC inputs
- One channels Stereo analog MUX
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

## Bluetooth

- Compliant with Bluetooth V5.1+BR+EDR+BLE specification
- Meet class1 class2 and class3 transmitting power requirement
- Support GFSK and π/4 DQPSK all packet types
- Provides maximum +8dbm@BDR, +6dbm@EDR transmitting power
- receiver with -94dBm@EDR sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile
- a2dp 1.3\avctp 1.4\avdtp 1.3\ avrcp 1.5\ hfp 1.5 \spp 1.0\rfcomm 1.2\pnp 1.3\ hid 1.0\sdp core4.2\l2cap core 4.2

## Peripherals

- One full speed USB 2.0 OTG controller
- One PCM/IIS for external digital Audio code, supports host and device mode
- Three SPI interface supports host and device mode
- Six multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex basic UART, support DMA mode
- One hard ware IIC interface supports host and device mode
- Built-in Cap Sense Key controller
- Two Built-in low power Cap Sense Keys
- 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIOs

## PMU

- Low voltage LDO and DC-DC for internal digital and analog circuit supply
- 2uA current consumption in the soft-off mode
- Built-in LDO and DC-DC for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 4.5V
- VDDIO is 2.2V to 3.4V

## Packages

- QFN32(4mm*4mm)

## Temperature

- Operating temperature: -40℃to+85℃
- Storage temperature: -65℃ to +150℃

## Applications

- Bluetooth TWS headse

# 1、Pin Definition

## 1.1 Pin Assignment

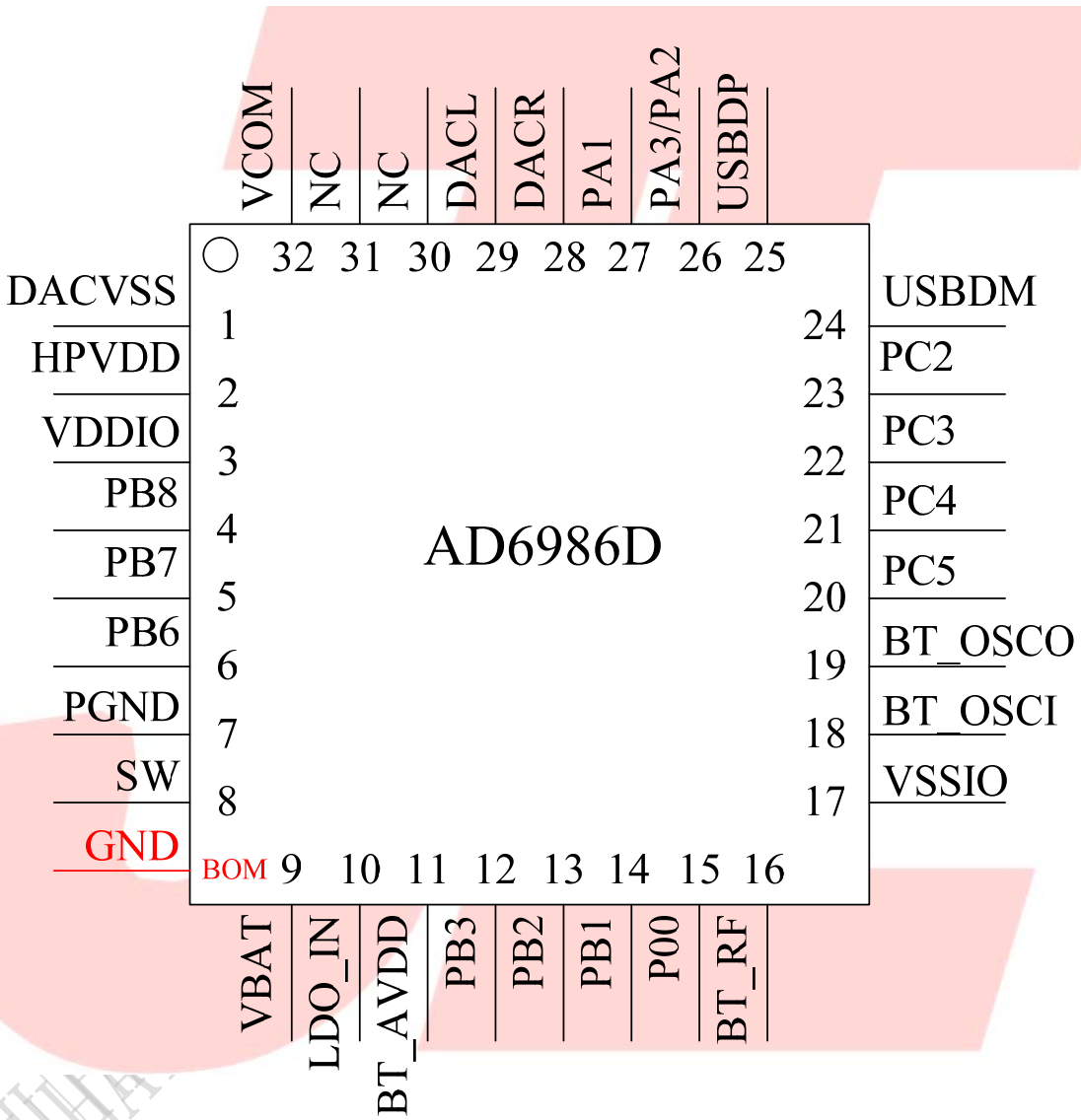



**Figure 1-1 AD6986D Package Diagram**

## 1.2 Pin Description

**Table 1-1 AD6986D Pin Description**

| PIN NO. | Name | I/O Type | Drive (mA) | Function | Other Function |
|---|---|---|---|---|---|
| 1 | DACVSS | P | / | | Analog Ground |
| 2 | HPVDD | P | / | | Headphone AMP Power |
| 3 | VDDIO | P | / | | IO Power 3.3v |
| 4 | PB8 | I/O | 8 | GPIO<br>(High Voltage Input) | UART0RXB：Uart0 Data Input(B)；<br>CAP4：Timer4 Capture； |
| 5 | PB7 | I/O | 8/24 | GPIO | UART0TXB：Uart0 Data Output(B);<br>SPI1DOA：SPI1 Data Out(A);<br>ADC8：ADC Input Channel 8；<br>Touch1：Touch Input Channel 1; |
| 6 | PB6 | I/O | 8/24 | GPIO | UART1RXA：Uart1 Data Input(A)；<br>SPI1CLKA：SPI1 Clk(A);<br>PWM2：Timer2 PWM Output；<br>ADC9：ADC Input Channel 9；<br>Touch7：Touch Input Channel 7; |
| 7 | PGND | P | / | | DCDC Ground |
| 8 | SW | P | / | | DCDC switch output, connected to inductor |
| 9 | VBAT | P | / | | Power Supply, connect to battery |
| 10 | LDO_IN | P | / | | Charge Power Input;<br>UART0TXC：Uart0 Data Output(C);<br>UART0RXC：Uart0 Data Input(C);<br>PWM3：Timer3 PWM Output；<br>CAP1：Timer1 Capture; |
| 11 | BT_AVDD | P | / | GPIO | BT Power |
| 12 | PB3 | I/O | 8/24 | GPIO | UART1TXB：Uart1 Data Output(B);<br>UART1RXB：Uart1 Data Input(B);<br>ALNK_MCLK(B)：ALNK Master Clock(B);<br>SPI2_DIC：SPI2 Data In(C);<br>TMR4：Timer4 Clock Input; |
| | EVDD | P | / | | EVDD：Supply volte to peripherals |
| 13 | PB2 | I/O | 8/24 | GPIO | UART2RXC：Uart2 Data Input(C);<br>SPI2DOC：SPI2 Data Out(C);<br>CAP5：Timer5 Capture;<br>ADC7：ADC Input Channel 7；<br>LP_TH1：Low Power Touch Channel 1 |

| | | | | | |
|---|---|---|---|---|---|
| 14 | PB1 | I/O | 8/24 | GPIO<br>(pull up) | Long Press Reset；<br>SPI2CLKC：SPI2 Clk(C);<br>UART2TXC：Uart2 Data Output(C)<br>ADC6：ADC Input Channel 6；<br>LP_TH0：Low Power Touch Channel 0 |
| 15 | P00 | I/O | 8 | GPIO<br>(High Voltage Input) | |
| 16 | BT_RF | / | / | | BT Antenna |
| 17 | VSSIO | P | / | | Ground |
| 18 | BT_OSCI | I | / | | BTOSC In |
| 19 | BT_OSCO | O | / | | BTOSC Out |
| 20 | PC5 | I/O | 8/24 | GPIO | UART2RXD：Uart2 Data Input(D);<br>SPI1DOB：SPI1 Data Out(B);<br>ALNK_DAT3(B)：Audio Link Data3(B);<br>IIC_SDA_B：IIC SDA(B)；<br>ADC5：ADC Input Channel 5； |
| 21 | PC4 | I/O | 8/24 | GPIO | UART2TXD：Uart2 Data Output(D);<br>SPI1CLKB：SPI1 Clock(B);<br>ALNK_DAT2(B)：Audio Link Data2(B);<br>IIC_SCL_B：IIC SCL(B)；<br>ADC4：ADC Input Channel 4；<br>PWM4：Timer4 PWM Output； |
| 22 | PC3 | I/O | 8/24 | GPIO | UART0RXD：Uart0 Data Input(D);<br>SPI1DIB：SPI1 Data In(B);<br>ALNK_LRCK(B)：Audio Link Word Select(B);<br>IIC_SDA_C：IIC SDA(C)；<br>TMR3：Timer3 Clock Input;<br>Touch5：Touch Input Channel 5; |
| 23 | PC2 | I/O | 8/24 | GPIO | UART0TXD：Uart0 Data Output(D);<br>SPI2DIB：SPI2 Data In(B);<br>ALNK_SCLK(B)：Audio Link Serial Clock(B);<br>IIC_SCL_C：IIC SCL(C)；<br>TMR1：Timer1 Clock Input;<br>Touch4：Touch Input Channel 4; |
| 24 | USBDM | I/O | 4 | USB Negative Data | UART1RXD：Uart1 Data Input(D)；<br>SPI2DOB：SPI2 Data Out(B);<br>IIC_SDA_A：IIC SDA(A)；<br>ADC11：ADC Input Channel 11； |
| 25 | USBDP | I/O | 4 | USB Positive Data | UART1TXD：Uart1 Data Output(D)；<br>SPI2CLKB：SPI2 Clock(B);<br>IIC_SCL_A：IIC SCL(A)； |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ADC10：ADC Input Channel 10； |
| 26 | PA3 | I/O | 8/24 | GPIO | UART2TXA：Uart2 Data Output(A);<br>ADC0：ADC Input Channel 0；<br>PWM1：Timer1 PWM Output；<br>Touch0：Touch Input Channel 0; |
| | PA2 | I/O | 8/24 | GPIO | UART1RXC：Uart1 Data Input(C)；<br>MIC_BIAS0：MIC0 Bias Output；<br>CAP3：Timer3 Capture; |
| 27 | PA1 | I/O | 8/24 | GPIO | MIC0：MIC0 Input Channel ;<br>PWM0：Timer0 PWM Output；<br>UART1TXC：Uart1 Data Output(C)； |
| 28 | DACR | O | / | | DAC Right Channel |
| 29 | DACL | O | / | | DAC Left Channel |
| 30 | NC | | | | |
| 31 | NC | | | | |
| 32 | VCOM | P | / | | DAC reference voltage |

# 2、Electrical Characteristics

## 2.1 Absolute Maximum Ratings

**Table** 2-1

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Topt | Operating temperature | -40 | +85 | ℃ |
| Tstg | Storage temperature | -65 | +150 | ℃ |
| VBAT | Supply Voltage | -0.3 | 4.5 | V |
| LDO_IN | Charger Voltage | -0.3 | 6 | V |
| $V_{3.3IO}$ | 3.3V IO Input Voltage | -0.3 | 3.6 | V |

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

## 2.2 PMU Characteristics

**Table** 2-2

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| VBAT | Voltage Input | 2.2 | 3.7 | 4.2 | V | |
| LDO_IN | Charger supply Voltage | 4.5 | 5.0 | 5.5 | V | |
| Normal mode | | | | | | |
| VDDIO | Voltage output | _ | 3.0 | _ | V | VBAT = 4.2V, 10mA loading |
| | Loading current | _ | _ | 100 | mA | VDDIO=3V@VBAT = 4.2V |
| BT_AVDD | Voltage output | _ | 1.25 | _ | V | VDDIO=3.0V, 10mA loading |
| | Loading current | _ | _ | 60 | mA | BT_AVDD=1.25V@VDDIO=3.0v |
| EVDD | Voltage output | _ | 1.1 | _ | V | BT_AVDD=1.25V, 1mA loading |
| | Loading current | _ | _ | 5 | mA | EVDD=1.1V@BT_AVDD=1.25v |
| LP mode | | | | | | |
| VDDIO | Loading current | | | 5 | mA | VDDIO=3V@VBAT = 4.2V |

## 2.3 Battery Charge

**Table 2-3**

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| LDO_IN | Charge Input Voltage | 4.5 | 5 | 5.5 | V | _ |
| $V_{Charge}$ | Charge Voltage | 4.15 | 4.2 | 4.25 | V | _ |

| | | | | | | |
|---|---|---|---|---|---|---|
| $I_{Charge}$ | Charge Current | 20 | | 200 | mA | Charge current at fast charge mode |
| $I_{Trikl}$ | Trickle Charge Current | 20 | 45 | 70 | mA | $V_{BAT}<V_{Trikl}$ |

## 2.4 IO Input/Output Electrical Logical Characteristics

**Table** 2-4

| **IO input characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| $V_{IL}$ | Low-Level Input Voltage | -0.3 | _ | 0.3* VDDIO | V | VDDIO = 3.3V |
| $V_{IH}$ | High-Level Input Voltage | 0.7* VDDIO | _ | VDDIO+0.3 | V | VDDIO = 3.3V |
| **IO output characteristics** | | | | | | |
| $V_{OL}$ | Low-Level Output Voltage | _ | _ | 0.33 | V | VDDIO = 3.3V |
| $V_{OH}$ | High-Level Output Voltage | 2.7 | _ | _ | V | VDDIO = 3.3V |

## 2.5 Internal Resistor Characteristics

**Table** 2-5

| **Port** | **General Output** | **High Drive** | **Internal Pull-Up Resistor** | **Internal Pull-Down Resistor** | **Comment** |
|---|---|---|---|---|---|
| PA1~PA3<br>PC2~PC5<br>PB0~PB2<br>PB6 PB7 | 8mA | 24mA | 10K | 10K | 1、PB1 default pull up<br>2、USBDM & USBDP default pull down<br>3、internal pull-up/pull-down resistance \| accuracy ±20% |
| PB0 PB8 | 8mA | _ | 10K | 10K | |
| USBDP | 4mA | _ | 1.5K | 15K | |
| USBDM | 4mA | _ | 180K | 15K | |

## 2.6 DAC Characteristics

**Table** 2-6

| **Parameter** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
|---|---|---|---|---|---|
| Frequency Response | 20 | _ | 20K | Hz | 1KHz/0dB<br>10Kohm loading<br>With A-Weighted Filter |
| THD+N | _ | -80 | _ | dB | |
| S/N | _ | 101 | _ | dB | |
| Crosstalk | _ | -80 | _ | dB | |
| Output Swing | | 0.45 | | Vrms | |
| Dynamic Range | | 95 | | dB | 1KHz/-60dB |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | 10Kohm loading<br>With A-Weighted Filter |
| DAC Output Power | _ | 6 | _ | mW | 32ohm loading |

## 2.7 ADC Characteristics

**Table** 2-7

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Dynamic Range | | 80 | | dB | 1KHz/-60dB |
| S/N | _ | 92 | _ | dB | 1KHz/-60dB |
| THD+N | _ | -72 | _ | dB | |
| Crosstalk | _ | -80 | _ | dB | |

## 2.8 BT Characteristics

### 2.8.1 Transmitter

**Basic Data Rate** **Table 2-8**

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RF Transmit Power | | | 6 | 8 | dBm | 25℃,<br>Power Supply<br>VBAT=5V<br>2441MHz |
| RF Power Control Range | | | 20 | | dB | |
| 20dB Bandwidth | | | 950 | | KHz | |
| Adjacent Channel Transmit Power | +2MHz | | -40 | | dBm | |
| | -2MHz | | -38 | | dBm | |
| | +3MHz | | -44 | | dBm | |
| | -3MHz | | -35 | | dBm | |

**Enhanced Data Rate** **Table 2-9**

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Relative Power | | | -1 | | dB | 25℃,<br>Power Supply<br>VBAT=5V<br>2441MHz |
| π/4 DQPSK Modulation Accuracy | DEVM RMS | | 6 | | % | |
| | DEVM 99% | | 10 | | % | |
| | DEVM Peak | | 15 | | % | |
| Adjacent Channel Transmit Power | +2MHz | | -40 | | dBm | |
| | -2MHz | | -38 | | dBm | |
| | +3MHz | | -44 | | dBm | |
| | -3MHz | | -35 | | dBm | |

### 2.8.2 Receiver

**Basic Data Rate** **Table 2-10**

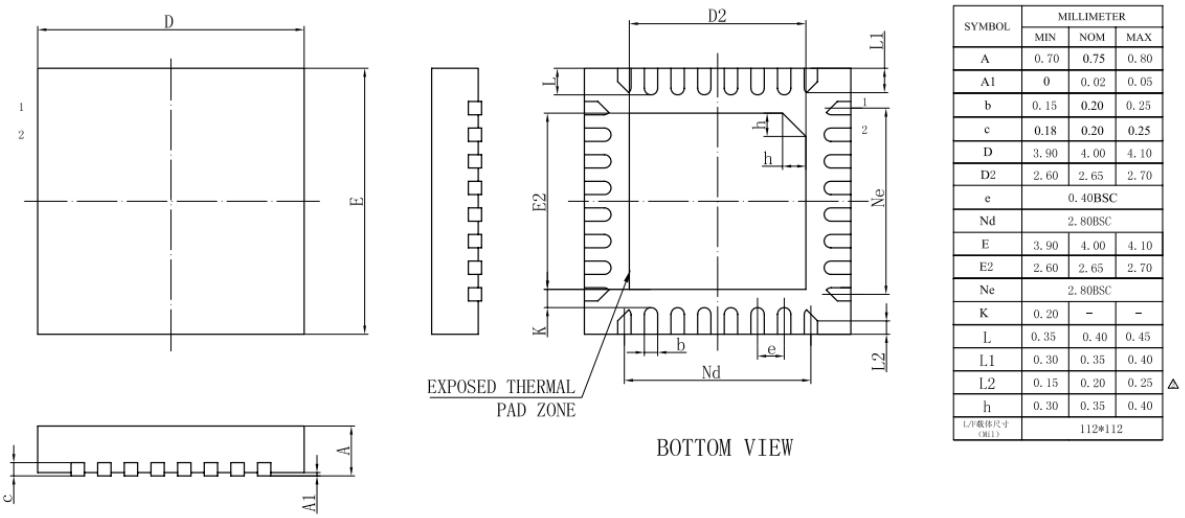
| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Sensitivity | | | -94 | | dBm | |
| Co-channel Interference Rejection | | | -13 | | dB | |
| Adjacent Channel Interference Rejection | +1MHz | | +5 | | dB | 25℃, Power Supply VBAT=5V 2441MHz |
| | -1MHz | | +2 | | dB | |
| | +2MHz | | +37 | | dB | |
| | -2MHz | | +36 | | dB | |
| | +3MHz | | +40 | | dB | |
| | -3MHz | | +35 | | dB | |

**Enhanced Data Rate** **Table 2-11**

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Sensitivity | | | -94 | | dBm | |
| Co-channel Interference Rejection | | | -13 | | dB | |
| Adjacent Channel Interference Rejection | +1MHz | | +5 | | dB | 25℃, Power Supply VBAT=5V 2441MHz |
| | -1MHz | | +2 | | dB | |
| | +2MHz | | +37 | | dB | |
| | -2MHz | | +36 | | dB | |
| | +3MHz | | +40 | | dB | |
| | -3MHz | | +35 | | dB | |

# 3、 Package Information

## 3.1 QFN32_4.0x4.0




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.60 | 2.65 | 2.70 |
| e | 0.40BSC | | |
| Nd | 2.80BSC | | |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.60 | 2.65 | 2.70 |
| Ne | 2.80BSC | | |
| K | 0.20 | – | – |
| L | 0.35 | 0.40 | 0.45 |
| L1 | 0.30 | 0.35 | 0.40 |
| L2 | 0.15 | 0.20 | 0.25 |
| h | 0.30 | 0.35 | 0.40 |
| L/F载体尺寸 (MIL) | 112*112 | | |

**Figure 3-1 AD6986D Package**

# 4、Revision History

| Date | Revision | Description |
|---|---|---|
| 2020.12.08 | V2.0 | Initial Release |
| | | |
| | | |
| | | |