
AD6983E Datasheet

Zhuhai Jieli Technology Co.,LTD

Version: 1.0

Date: 2021.01.29

Copyright © Zhuhai Jieli Technology Co.,LTD. All rights reserved.

AD6983E Features

CPU

- 32-bit DSP supports hardware Float Point Unit(FPU)
- Up to 160MHz programmable processor
- 64Vectored interrupts
- 4 Levels interrupt priority

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC,AES)
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 20-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC, SNR >= 101dB
- Two channels 24-bit ADC , SNR>=90dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- One analog MIC amplifier, build-in MIC bias generator
- Supports two PDM digital MIC inputs
- One channel Stereo analog MUX
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth

V5.1+BR+EDR+BLE specification

- Meet class1 class2 and class3 transmitting power requirement
- Support GFSK and $\pi/4$ DQPSK all packet types
- Provides maximum +8dbm@BDR, +6dbm@EDR transmitting power
- receiver with -94dBm@EDR sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap gatt\rfcomm\sdp\l2cap profile
- a2dp 1.3\avctp 1.4\avdtp 1.3\avrcp 1.5\hfp 1.5 \spp 1.0\rfcomm 1.2\pnp 1.3\hid 1.0\sdp core4.2\l2cap core 4.2

Peripherals

- One full speed USB 2.0 OTG controller
- Six multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex basic UART, support DMA mode
- One hardware IIC interface supports host and device mode
- Two Built-in low power Cap Sense Keys
- Built-in Cap Sense Key controller
- 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIOs

PMU

- Low voltage LDO for internal digital and analog circuit supply
- 2uA current consumption in the soft-off mode
- Built-in LDO for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 4.5V
- VDDIO is 2.2V to 3.4V

Packages

- QFN20(3mm*3mm)

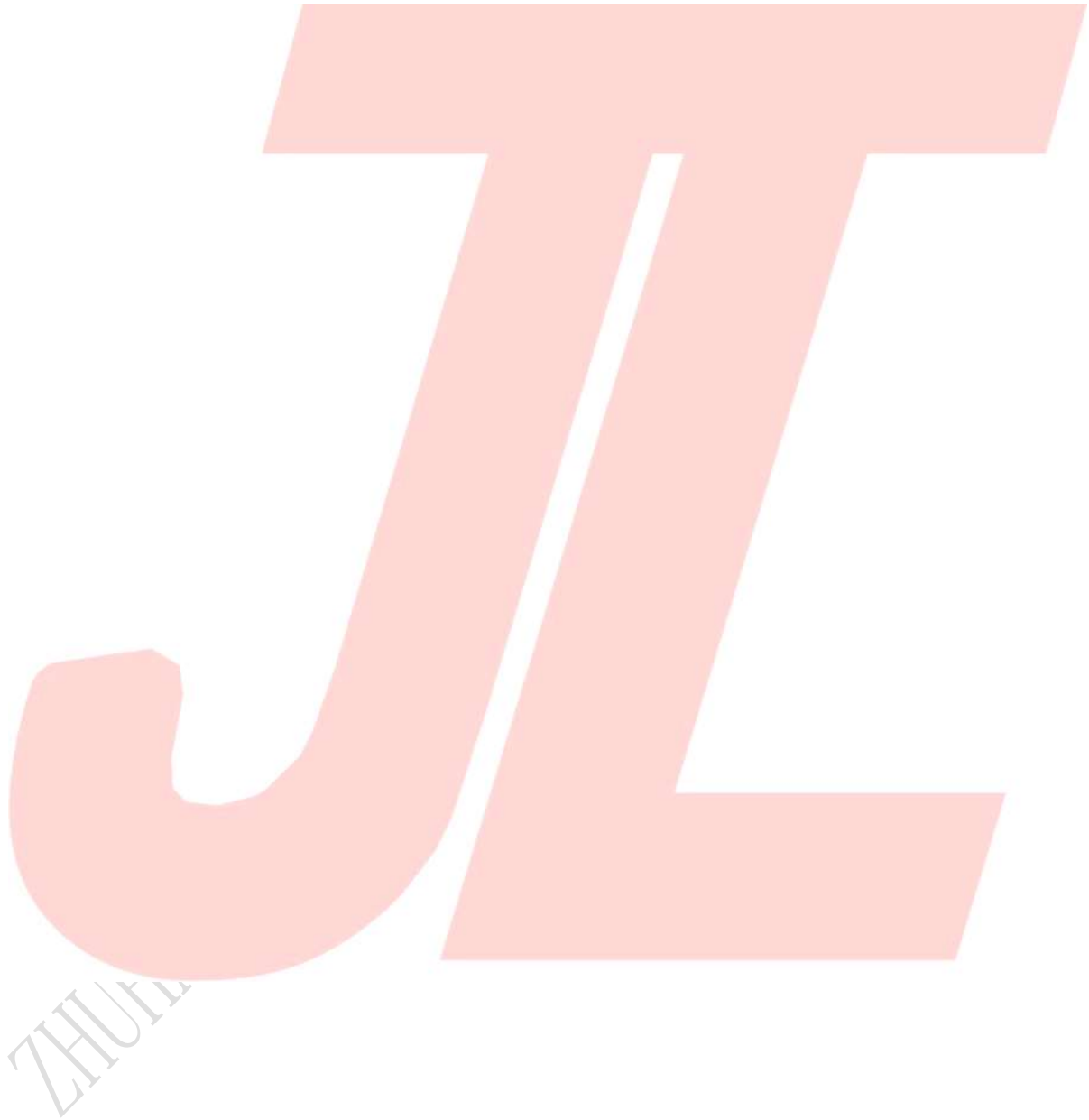
● Storage temperature: -65°C to +150°C

Temperature

● Operating temperature: -40°C to +85°C

Applications

● Bluetooth TWS Headset



Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

1、 Pin Definition

1.1 Pin Assignment

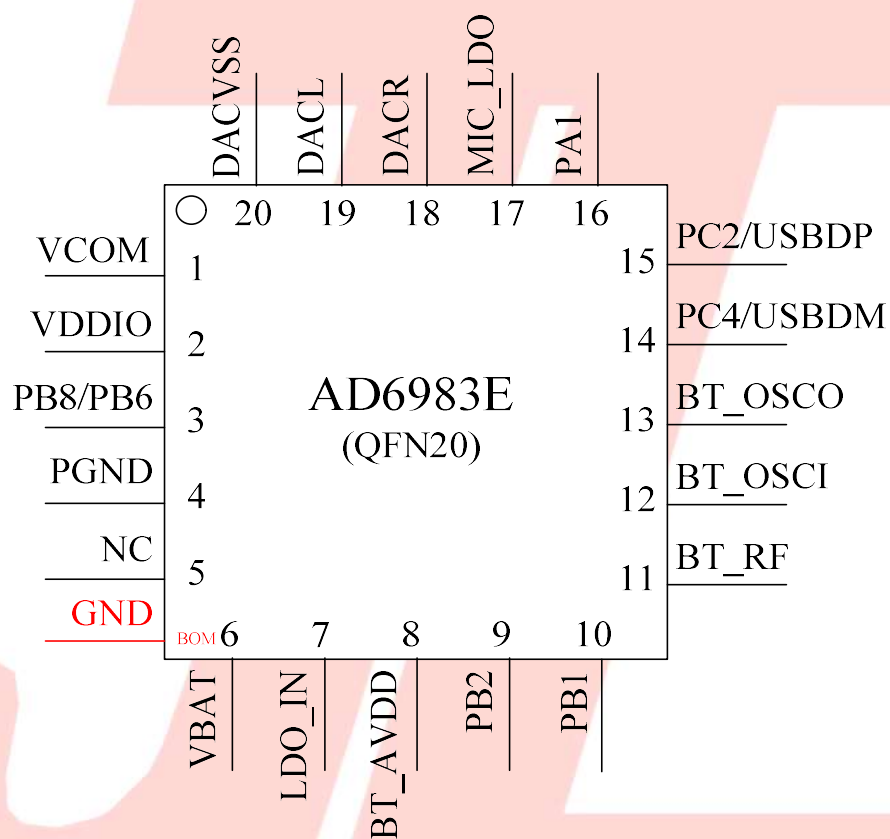


Figure 1-1 AD6983E Package Diagram

1.2 Pin Description

Table 1-1 AD6983E Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	VCOM	P	/		DAC reference voltage
2	VDDIO	P	/		IO Power 3.3v
3	PB8	I/O	8	GPIO	UART0RXB: Uart0 Data Input(B); CAP4: Timer4 Capture;
	PB6	I/O	8/24	GPIO	UART1RXA: Uart1 Data Input(A); PWM2: Timer2 PWM Output; ADC9: ADC Input Channel 9; Touch7: Touch Input Channel 7;
4	PGND	P	/		DCDC Ground
5	NC	/	/		
6	VBAT	P	/		Connect to battery
7	LDO_IN	P	/		Charge Power Input; UART0TXC: Uart0 Data Output(C); UART0RXC: Uart0 Data Input(C); PWM3: Timer3 PWM Output; CAP1: Timer1 Capture;
8	BT_AVDD	P	/		BT Power
9	PB2	I/O	8/24	GPIO	UART2RXC: Uart2 Data Input(C); CAP5: Timer5 Capture; ADC7: ADC Input Channel 7; LP_TH1: Low Power Touch Channel 1
10	PB1	I/O	8/24	GPIO (pull up)	Long Press Reset; UART2TXC: Uart2 Data Output(C) ADC6: ADC Input Channel 6; LP_TH0: Low Power Touch Channel 0
11	BT_RF	/	/		BT Antenna
12	BT_OSCI	I	/		BTOSC In
13	BT_OSCO	O	/		BTOSC Out
14	PC4	I/O	8/24	GPIO	UART2TXD: Uart2 Data Output(D); IIC_SCL_B: IIC SCL(B); ADC4: ADC Input Channel 4; PWM4: Timer4 PWM Output;
	USBDM	I/O	4	USB Negative Data	UART1RXD: Uart1 Data Input(D); IIC_SDA_A: IIC SDA(A);

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

					ADC11: ADC Input Channel 11;
15	USBDP	I/O	4	USB Positive Data	UART1TXD: Uart1 Data Output(D); IIC_SCL_A: IIC SCL(A); ADC10: ADC Input Channel 10;
	PC2	I/O	8/24		IIC_SCL_C: IIC SCL(C); UART0TXD: Uart0 Data Output(D); TMR1: Timer1 Clock Input;
16	PA1	I/O	8/24	GPIO	MIC0: MIC0 Input Channel ; PWM0: Timer0 PWM Output; UART1TXC: Uart1 Data Output(C);
17	MIC_LDO	P	/		MIC Power
18	DACR	O	/		DAC Right Channel
19	DACL	O	/		DAC Left Channel
20	DACVSS	P	/		Analog Ground

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
LDO_IN	Charger Voltage	-0.3	6	V
V _{3.3IO}	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.2	V	
LDO_IN	Charger supply Voltage	4.5	5.0	5.5	V	
Normal mode						
VDDIO	Voltage output	–	3.0	–	V	VBAT = 4.2V, 10mA loading
	Loading current	–	–	100	mA	VDDIO=3V@VBAT = 4.2V
BT_AVDD	Voltage output	–	1.25V	–	V	VDDIO=3.0V, 10mA loading
	Loading current	–	–	60	mA	BT_AVDD=1.25V@VDDIO=3.0v
LP mode						
VDDIO	Loading current			5	mA	VDDIO=3V@VBAT = 4.2V

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDO_IN	Charge Input Voltage	4.5	5	5.5	V	–
V _{Charge}	Charge Voltage	4.15	4.2	4.25	V	–
I _{Charge}	Charge Current	20		200	mA	Charge current at fast charge mode

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

I_{Trickl}	Trickle Charge Current	20	45	70	mA	$V_{\text{BAT}} < V_{\text{Trickl}}$
---------------------	------------------------	----	----	----	----	--------------------------------------

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Low-Level Input Voltage	-0.3	–	$0.3 * V_{\text{DDIO}}$	V	$V_{\text{DDIO}} = 3.0\text{V}$
V_{IH}	High-Level Input Voltage	$0.7 * V_{\text{DDIO}}$	–	$V_{\text{DDIO}} + 0.3$	V	$V_{\text{DDIO}} = 3.0\text{V}$
IO output characteristics						
V_{OL}	Low-Level Output Voltage	–	–	0.3	V	$V_{\text{DDIO}} = 3.0\text{V}$
V_{OH}	High-Level Output Voltage	2.7	–	–	V	$V_{\text{DDIO}} = 3.0\text{V}$

2.5 Internal Resistor Characteristics

Table 2-5

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA1, PB1,PB2, PB6 PC2,PC4	8mA	24mA	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull down 3、internal pull-up/pull-down resistance accuracy $\pm 20\%$
PB8	8mA	-	10K	10K	
USBDP	4mA	–	1.5K	15K	
USBDM	4mA	–	180K	15K	

2.6 DAC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	–	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	–	-80	–	dB	
S/N	–	101	–	dB	
Crosstalk	–	-80	–	dB	
Output Swing		0.45		Vrms	
Dynamic Range		95		dB	1KHz/-60dB 10Kohm loading

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

					With A-Weighted Filter
DAC Output Power	–	6	–	mW	32ohm loading

2.7 ADC Characteristics

Table 2-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		80		dB	1KHz/-60dB
S/N	–	92	–	dB	1KHz/-60dB
THD+N	–	-72	–	dB	
Crosstalk	–	-80	–	dB	

2.8 BT Characteristics

2.8.1 Transmitter

Basic Data Rate

Table 2-8

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		6	8	dBm	25°C, Power Supply VBAT=3.7V 2441MHz
RF Power Control Range		20		dB	
20dB Bandwidth		950		KHz	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Enhanced Data Rate

Table 2-9

Parameter	Min	Typ	Max	Unit	Test Conditions
Relative Power		-1	-3	dB	25°C, Power Supply VBAT=3.7 2441MHz
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS	6		%	
	DEVM 99%	10		%	
	DEVM Peak	15		%	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2.8.2 Receiver

Basic Data Rate

Table 2-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25°C, Power Supply VBAT=3.7 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel	+1MHz		+5		dB	
	-1MHz		+2		dB	
Interference Rejection	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Enhanced Data Rate

Table 2-11

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25°C, Power Supply VBAT=5V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel	+1MHz		+5		dB	
	-1MHz		+2		dB	
Interference Rejection	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

3、 Package Information

3.1 QFN20_3.0x3.0

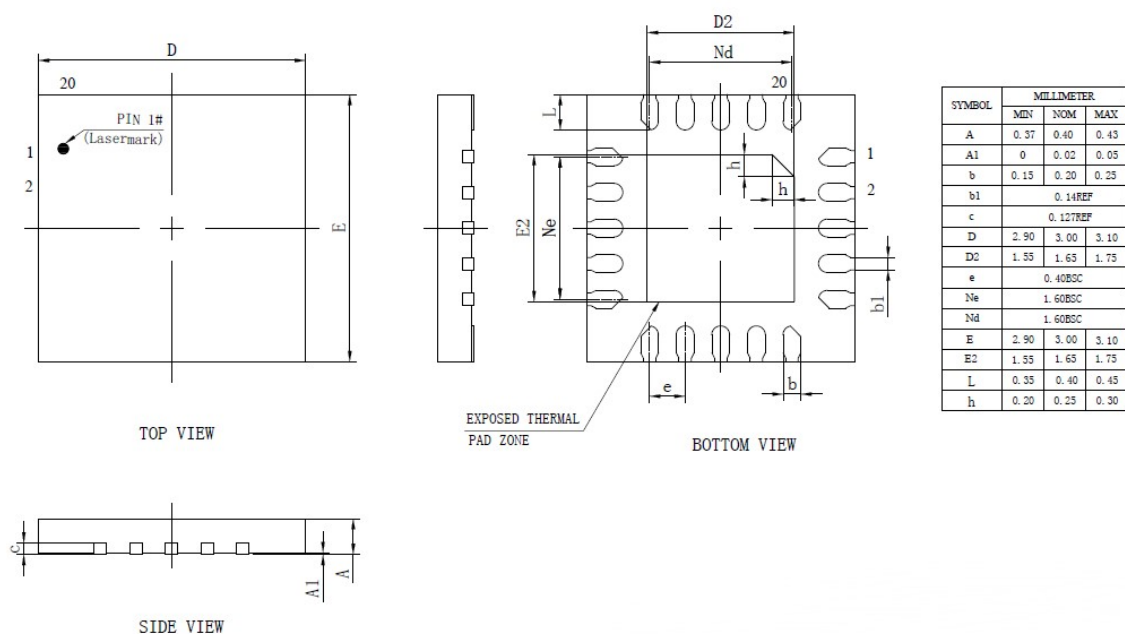


Figure 3-1 AD6983E Package

4、 Revision History

Date	Revision	Description
2021.03.29	V1.0	Initial Release

ZHUO

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.